INFORMATION DISCLOSURE STATEMENT BY APPLICANT PTO FORM 1449	Atty. Docket No. 10191/4188	Serial No. To Be Assigned
		10/539495
	Applicant(s) HARTER et al.	
	Filing Date Herewith	Group To Be Assigned

U. S. PATENT DOCUMENTS

EXAMINER'S INITIALS	PATENT NUMBER	PATENT DATE	NAME	CLASS	SUBCLASS	FILING DATE

FOREIGN PATENT DOCUMENTS

EXAMINER'S INITIALS	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION YES	NO

OTHER DOCUMENTS

EXAMINER'S INITIALS		AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.
/JPT/		Built-In Test for VLSI: Pseudorandom Techniques by Paul H. Bardell, William H. McAnney and Jacob Savir; pp. 124 et seq.*
/JPT/		A Linear Code-Preserving Signature Analyzer COPMISR; Hlawiczka et al; VLSI Test Symposium, 1997 – 15th IEEE Monterey, CA USA 27 April – 1 May 1997.; pp. 350-355.**
/JPT/		Low Cost BIST for EDAC Circuits; Badura et al; Test Symposium, 1997 (ATS '97), Proceedings, Sixth Asian Akita, Japan 17-19 November 1997; pp. 410-415.**
/JPT/		Utilization of On-Line (Concurrent) Checkers During Built-In-Self-Test and Vice Versa; Gupta et al.; IEEE Transactions on Computers; 1 January 1996; pp. 63-73.**
/JPT/		Design of t-UED/AUED Codes from Berger's AUED Code; Biswas et al.; VLSI Design, 1997, Proceedings, Tenth International Conference on Hyderabad; 4-7 January 1997; pp. 364-369.**

EXAMINER	/John P Trimmings/	DATE CONSIDERED 09/13/2007

EXAMINER: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

*Described in specification.
**Copy of reference is not enclosed because reference is cited in Search Report (copy of reference provided by International Searching Authority).